# Power Quality Improvement of DC Drive by Reduction of Circulating Current

<sup>1</sup>Rashi Goswami, <sup>2</sup>Anand Goswami

<sup>1</sup>Research scholar, Fourth Semester ME (Control System), <sup>2</sup>ME (Control System), Jabalpur Engineering College Jabalpur (M.P) 482011, India

*Abstract:* The paper presents power quality improvement of DC drives by reduction of circulating current in parallal operation of active filters based on hysteresis current control. As it is a well-known fact that power quality determines the fitness of electrical power to consumer devices, hence an effort has been made to improve power quality in this work. Simulation with the help of MATLAB/Simulink has been done and results obtained are discussed in detail to verify the theoretical results. The multipulse converter was connected with DC drives and was run at no load condition to find out the transient and steady state performances. FFT analysis has been performed and Total Harmonic Distortion (THD) results obtained at different pulses are shown here.

Keywords: Active Filter, Power Quality, Zero sequence circulating current, hysteresis control, Capacity enhancement.

#### I. INTRODUCTION

The power quality, at all time, is a matter of concern where a number of non-linear, harmonics producing and sophisticated loads are connected in a electrical distribution network. In that case Active Filters is finding greater applications for power quality (PQ) improvement. In many applications, the filtering task cannot be performed for the whole spectrum of harmonics by using a single converter due to the limitations on switching frequency and power rating of the semiconductor devices. Therefore, compensating the non-active components to improve the power quality as well as to avoid the large capacity centralised Active Filters, parallel operation of multiple low power AFsh units are increasing. Different controlling mechanism and topologies are available in handling the difficulties of parallel operation of AFsh either in active load sharing or distributed mode. A detailed technical review on parallel operation of APFsh for current and voltage harmonic compensation in a distributed generation (DG) network have been done in [1,2] where the pros and cons of the different control methods have been discussed. Fo r these cases, there is no physical/electrical link between the AFsh units. The system components and cost can be reduced by maintaining a common DC link back-to back connection between the AFsh units [3]. But it then raises the control complexity by introducing the zero sequence circulating current (ZSCC) flow within the AFsh units [4,5].

Most of the control methods for the reduction of ZSCC discussed in the literature are mainly for PWM based multiple inverter or rectifier units [6-10]. Very few of the articles show the ZSCC reduction for the parallel operation of AFsh units [11]. None of these discuss the ZSCC flow issues and control method for the parallel operation of Converter/AFsh based on hysteresis control. Therefore, an attempt has been made here to discuss the issues related to hysteresis control.

# **II. WORKING PRINCIPLE**

According to the working principle of an AFsh unit in parallel to the load to compensate harmonic current, there are two possible modes of operation: capacitive mode (where the current flows from the capacitor) and inductive mode (the current flows towards the capacitor). When multiple AF units work in a current sharing mode, there could be four possible modes of operation: (i) capacitive-capacitive, (ii) inductive-inductive, (iii)capacitive inductive and (iv) inductive-capacitive. As an example, Fig 1 shows a single line diagram of a system where  $i_{cc}$  represents the circulating current flow

between the AF units. In the case of this system this circulating current flow exists as a zero sequence harmonics in the zero sequence current flow when a circulating loop is created within the AFsh units and hence it is termed zero sequence circulating current (ZSCC) flow. In general these harmonics are (3+n\*6) order, where n = 0, 1, 2...

## **III. MODEL FOR ZSCC FLOW**

For simplicity, derivation of ZSCC flow has been carried out on a per phase basis. Fig 2 shows the possible mode of operation between the AFsh units where *sh-i* and *sh-c* represent the inductive and capacitive mode respectively. If there is a difference in any of the parameters, such as switching frequency, interfacing inductor, hysteresis band (in hysteresis current controller) then the AFsh units can operate in inductive-capacitive or capacitive-inductive mode. In these cases, ZSCC will flow and these are reflected in Fig 2 (f, h).

From Fig 2 (a and b), during the capacitive mode, the current flow can be obtained as;

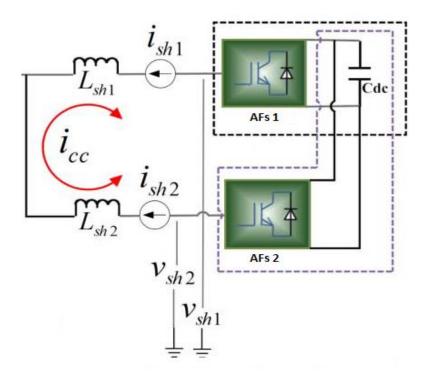


Fig 1: Single line diagram of a 2 units AFsh with common DC-link presenting CC flow

The high-level schematic shown in fig 2 is built from six main blocks. The DC motor, the two three-phase full converters, and the bridge firing unit are provided with the SimPower Systems library. More details on these blocks are available in the reference pages for each block. The two other blocks are specific to the Electric Drives library. These blocks are the speed controller and the current controller. They allow speed or torque regulation. A "regulation switch" block allows you to toggle from one type of regulation to the other. During torque regulation the speed controller is disabled. It is possible to use a simplified version of the drive containing an average-value model of the three-phase dual-converter and allowing faster simulation.

## SPEED CONTROLLER:

The speed regulator shown below uses a PI controller. The controller outputs the armature current reference (in pu) used by the current controller in order to obtain the electromagnetic torque needed to reach the desired speed. During torque regulation, the speed controller is disabled. The controller takes the speed reference (in rpm) and the rotor speed of the DC machine as inputs. The speed reference change rate will follow user-defined acceleration and deceleration ramps in order to avoid sudden reference changes that could cause armature over-current and destabilize the system. The speed measurement is filtered by a first-order low-pass filter.

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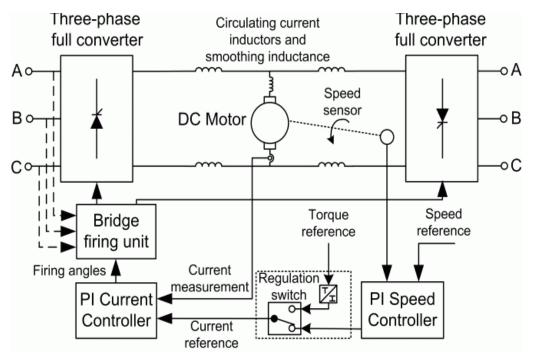


Fig 2 Block diagram of circulating current Controller

## **Current Controller:**

The armature current regulator shown below is based on a second PI controller. The regulator controls the armature current by computing the appropriate thyristor firing angles of the two full converters. This generates the converter output voltages needed to obtain the desired armature current and thus the desired electromagnetic torque. The controller takes the current reference (in pu) and the armature current flowing through the motor as inputs. The current reference is either provided by the speed controller during speed regulation or computed from the torque reference provided by the user during torque regulation. This is managed by the "regulation switch" block. The armature current input is filtered by a first-order low-pass filter. An arccosine function is used to linearize the control system. The firing angle can vary between 0 and 180 degrees. You can limit the lower and upper limits to intermediate values. Both converters operate simultaneously, and the two firing angles are controlled so that the sum of their values stays equal to 180 degrees. This produces opposite average voltages at the converter DC output terminals and thus identical average voltages at the DC motor armature, the converters being connected in antiparallel. One converter is working in rectifier mode while the other is in inverter mode.

#### **Circuit Description:**

This circuit is based on the DC4 block of Sim Power Systems It models a four-quadrant three-phase rectifier (dualconverter topology) drive with no circulating current for a 200 HP DC motor.

The 200 HP DC motor is separately excited with a constant 310 V DC field voltage source. The armature voltage is provided by two three-phase anti-parallel connected converters controlled by two PI regulators. This allows bidirectionnal current flow through the DC motor armature circuit and thus four-quadrant operation. The converters are fed by a 380 V AC 50 Hz voltage source.

The regulators control the firing angles of both converter thyristors. The first regulator is a speed regulator, followed by a current regulator. The speed regulator outputs the armature current reference (in p.u.) used by the current controller in order to obtain the electromagnetic torque needed to reach the desired speed. The speed reference change rate follows acceleration and deceleration ramps in order to avoid sudden reference changes that could cause armature over-current and destabilize the system. The current regulator controls the armature current by computing the appropriate thyristor firing angles. This generates the converter output voltages needed to obtain the desired armature currents.

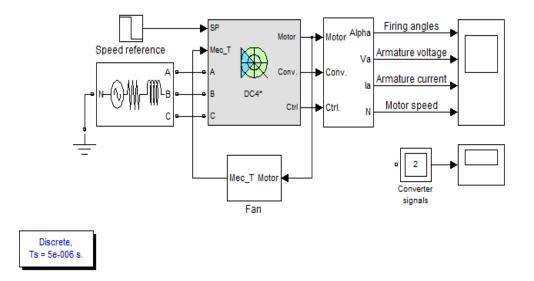
The output of universal bridge, which is DC power is fed to DC motor having the following ratings.

Power = 5 HP = 3.73 kW

Voltage = 240 V

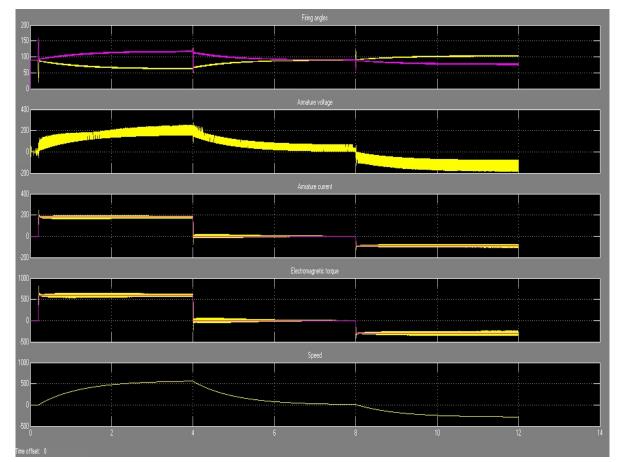
Speed = 1500rpm

In Circulating Current Mode:



#### Fig 3. Block Diagram of Circulating Current Mode

**D** C Motor Characterstics in Circulating Current Mode:



# In Non Circulating Current Mode:

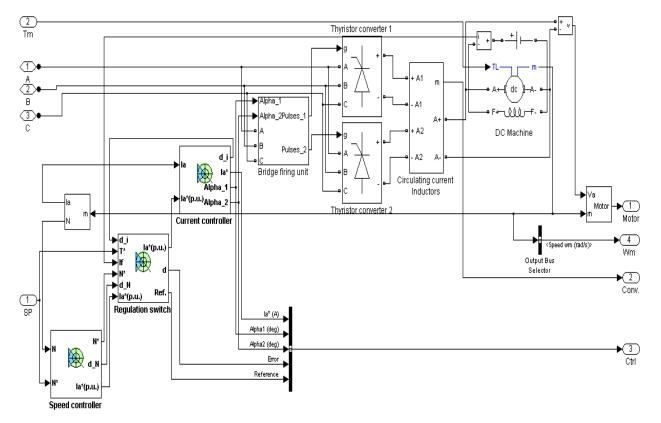
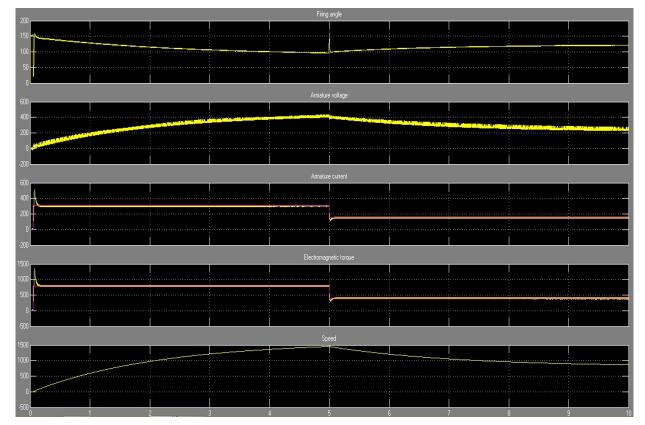


Fig 4 Block Diagram In Non Circulating CurrentMode

D C Motor Characteristics In Non Circulating Current Mode:



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| Туре                                       | THD    | Settling time | Voltage ripple | Current ripple |
|--------------------------------------------|--------|---------------|----------------|----------------|
|                                            |        | (s)           | V              | А              |
| Without Filter                             | 78.33% | 4s            | 20 V           | 5A             |
| With Filter (circulating current Mode)     | 62.68% | 3s            | 12V            | 3.75A          |
| Filter with Circulating Current controller | 8.95%  | 1s            | 3V             | 2.11A          |

# **IV. CONCLUSION**

In this paper a performance comparison of power quality improvement of DC drives by reduction of circulating current based on hysteresis current control multi pulse converter has been modeled and simulated in MATLAB/Simulink. The results obtained are analyzed and it is proved that in case of non-circulating mode THD decreases, settling time decreases, Output Voltage and current ripple also decreases considerably.

## REFERENCES

- S. K. Khadem, M. Basu and M. F. Conlon, "A review of paralleloperation of active power filters in the distributed generation system,"Power Electronics and Applications (EPE 2011), Proceedings of the2011-14th European Conference on , vol., no., pp.1-10, Aug. 30 2011-Sept. 1 2011
- [2] S. K. Khadem, M. Basu and M. F. Conlon, "Parallel Operation of Inverters and Active Power Filters in Distributed Generation System aReview", Renewable and Sustainable Energy Reviews, vol.15, 2011, pp. 5155–5168
- [3] H Akagi and K Nabae, Control strategy of active power filters usingmultiple voltage source PWM converters, IEEE Trans. Ind. Appl. 1(3)(1985), pp. 460–466
- [4] L Asiminoaei, E Aeloiza, J Kim, P H Enjeti, F Blaabjerg, L Moran, SSul, Parallel Interleaved Inverters for Reactive Power and HarmonicCompensation, PESC, (2006), pp.1-7
- [5] L Asiminoaei, C. Lascu, Performance Improvement of Shunt Active Power Filter With Dual Parallel Topology, IEEE Trans Power Electronics 22(1) (2007), pp. 247-259
- [6] Z Ye, D Boroyevich, J Y Choi and F C Lee, Control of circulating current in parallel three-phase boost rectifiers, IEEE APEC (2000), pp. 506–512.
- [7] Chen, T P, Circulating zero-sequence current control of parallel threephase inverters, Electric Power Applications, vol.153, no.2, pp. 282-288, 2006
- [8] C T Pan and Y H Liao, Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers, IEEE Trans. Ind. Electron. 54(2) (2007), pp. 825–838.